AMENDMENT TO THE SPECIFICATION

Please amend paragraph [0030] of the Specification as follows:

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[0030] Referring to FIG. 2, an AES encryption/decryption apparatus according to the present invention includes a key schedule unit 202 receiving 128/192/256 bit keys so as to be in charge of a key schedule, a block round unit 203 receiving 128 block data so as to carry out encryption/decryption, and a control unit 201, such as a processor, generating control signals required for the key schedule unit 202 and the block round unit 203 and receiving to convert a stream of a byte unit into that of a block unit through an input buffer to output the converted stream to the block round unit 203 or converting block data outputted from the block round unit 203 into byte units so as to output the converted byte units externally.

AMENDMENT TO THE SPECIFICATION

Please amend paragraph [0049] of the Specification as follows:

[0050] In this case, the encryption/decryption key required for each round is inputted from the key schedule unit 202. Moreover, the block round unit 203 carries out the calculation of all rounds before the next block data is transferred from the control unit 201. This is because the hardware structure that the control unit 201, key schedule unit 202, and block round unit 203 are preferably constructed with logic gates so as to enable a real-time processing. Alternatively, other programmable logic devices ~~or software processing~~ known to one of ordinary in the art may also be substituted.

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